

Amendments to the Specification:

Please replace the paragraph beginning at page 4, line 8, with the following rewritten paragraph:

B1
--In FIG. 1, sensor 10 is formed in substrate 12 of a first conductivity type (preferably p) in a first concentration (preferably p^-). Sensor 10 includes CMOS circuitry 30 to control the sensor and further includes first well 14 of the first conductivity type in a second concentration (preferably p) formed in substrate 12. The second concentration (preferably p) is greater than the first concentration (preferably p^-). Sensor 10 further includes photodiode region 16 of a second conductivity type (preferably n) formed in the first well. Sensor 10 further includes pinning layer 18 of the first conductivity type (preferably p) formed to a shallow depth in the photodiode region and electrically coupled to the substrate. Preferably, pinning layer 18 is doped to a higher concentration (preferably p^+) than a concentration of the first well.--

Please replace the paragraph beginning at page 5, line 1, with the following rewritten paragraph:

B2
--Similarly, in FIG. 2, sensor 40 is formed in substrate 42 of a first conductivity type (preferably p) in a first concentration (preferably p^-). Sensor 40 includes CMOS circuitry 60 to control the sensor and further includes first well 44 of the first conductivity type in a second concentration (preferably p) formed in the substrate. The second concentration (preferably p) is greater than the first concentration (preferably p^-). Sensor 40 further includes photodiode region 46 of a second conductivity type (preferably n) formed in the first well. Sensor 40 further includes pinning layer 48 of the first conductivity type (preferably p) formed to a shallow depth in the photodiode region and electrically coupled to the substrate. Preferably, pinning layer 48 is doped to a higher concentration (preferably p^+) than a concentration of the first well.--

Please replace the paragraph beginning at page 5, line 25, with the following rewritten paragraph:

B3
--In FIG. 3, sensor 70 is formed in substrate 72 of a first conductivity type (preferably p) in a first concentration (preferably p^-). Sensor 70 includes CMOS circuitry 90 to control the

B3 sensor and further includes first well 74 of the first conductivity type in a second concentration (preferably p) formed in substrate 72. The second concentration (preferably p) is greater than the first concentration (preferably p⁻). Sensor 70 further includes photodiode region 76 of a second conductivity type (preferably n) formed in the first well.--

Please replace the paragraph beginning at page 8, line 8, with the following rewritten paragraph:

B4 --The present invention takes advantage of a customary CMOS process. In particular, a p well (32, 62, 92) is used in the conventional CMOS process beneath n-FETs (34, 64, 94) to adjust the behavior of the n-FETs (e.g., to achieve a useful threshold voltage V_T). The inventor discovered that this same p well customarily used in the CMOS process, in the same implant cycle as used in the CMOS process, can also be used to form p-region 14, 44 or 74 in FIG. 1, 2 or 3. There is no need to add any additional processes. The inventor discovered that the customary CMOS p well implant beneath n-FETs also produces a barrier that can reduce cross talk in four transistor pixels and five transistor pixels.--

Please replace the paragraph beginning at page 8, line 16, with the following rewritten paragraph:

B5 --In an alternative variant, the p implant beneath the photodiode is increased in dose and/or depth to produce a higher barrier when needed. This increased dose and/or depth (see FIGS. 7, 8, 9) would require an extra implant process above and beyond the conventional CMOS p well implant process.--

Please replace the paragraph beginning at page 9, line 5, with the following rewritten paragraph:

B6 --In an alternative embodiment, a lightly doped p⁻ type epi (13, 43, 73 of FIGS. 10, 11, 12) is grown on a more heavily doped p⁺ type substrate. The p⁺ type substrate is typically several hundred micron thick, and the p⁻ type epi is typically several microns deep. Then, the p well (e.g., p-region 14, 44 or 74 in FIGS. 1, 2 or 3-10, 11, 12) is formed in the p⁻ type epi, but only so deep as to extend down a few microns into the p⁻ type epi. In operation, any electron that ventures into, or is photo formed in, the heavily doped p⁺ type substrate recombines almost

36 immediately with holes (i.e., the majority carrier in the p^+ type substrate) due to the heavy concentration of dopant ions. These electrons never have a chance to diffuse back into the p^- type epi and then potentially into the storage well that is the photodiode. Meanwhile, the p well barrier (e.g., p-region 14, 44 or 74 in FIGS. ~~1, 2 or 3~~ 10, 11, 12) prevents any free charge in the p^- type epi region from diffusing into the storage well.--
